REMARKS/ARGUMENTS

In the Office action dated November 1, 2005, claims 1 – 22 were rejected. Applicant hereby requests reconsideration of the application in view of the below-provided remarks.

I. Priority Document

Applicant encloses herewith a Certified Copy of the Priority Document no. 200203823-0, a patent application filed in Singapore on June 25, 2002.

II. Objection to the Specification

The Specification is objected to because it does not include a statement of the field of art to which the invention pertains. Applicant asserts that a statement as to the field of the invention is not required by statute or regulation. Therefore, a statement of the field has not been included.

III. Claim Rejections

Claims 1 – 6, 8 – 11, 13 – 18, and 20 – 22 were rejected under 35 U.S.C. 102(b) as being anticipated by Gilley (U.S. Pat. No. 6,215,876).

Claim 1

Claim 1 recites:

> "A bit error detection circuit comprising:
> a predictor circuit ***that uses a plurality of bits of a bit sequence to predict a next bit in the sequence***;
> a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; and
> a correction circuit ***that corrects any error in the actual next bit to provide a corrected actual next bit***." (emphasis added)

With regard to claim 1, the Office action states that Gilley teaches all of the elements of claim 1. In particular, the Office cites:

1) Figure 4, #60 and column 6, lines 43 – 46 as anticipating the predictor circuit; and

2) Figure 4, #78 and column 7, lines 1 – 5 as anticipating the correction circuit.

Gilley does not disclose a ***predictor circuit*** as recited in claim 1

Applicant points out that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) [MPEP 2131]

The predictor circuit recited in claim 1 "***uses a plurality of bits of a bit sequence to predict a next bit in the sequence***." At column 6, lines 43 – 45, Gilley discloses receiving an initialization vector (IV) "and simultaneously predict*[ing]* what IV for that moment should be." Similarly, in Fig. 4, element 60, Gilley discloses the phrase "predict IV." While Gilley discloses the general concept of predicting an initialization vector, nowhere in the cited passage of column 6, lines 46 – 49 does Gilley disclose a predictor circuit or a prediction technique that "uses a plurality of bits of a bit sequence to predict a next bit in the sequence" as recited in claim 1. Further, Applicant asserts that the limitations of the predictor circuit are not disclosed anywhere else by Gilley. Because Gilley does not disclose each and every element of the predictor circuit as recited in claim 1, claim 1 is not anticipated by Gilley.

Gilley does not disclose a ***correction circuit*** as recited in claim 1

The correction circuit recited in claim 1 "***corrects any error in the actual next bit to provide a corrected actual next bit***." The correction circuit of claim 1 is deemed to be anticipated by Gilley at Fig. 4, #78 and column 7, lines 1 – 5. In Fig. 4 of Gilley, element 78 is an action that is taken when the number of bit errors is greater than or equal to four. If the number of bit errors is greater than or equal to four, then it is assumed that the predicted initialization vector is wrong (element 76) and element 78 simply recites "decide further action." The statement "decide further action" does not disclose a correction circuit "that corrects any error in the actual next

bit to provide a corrected actual next bit." At column 7, lines 1 – 5, Gilley describes the process related to element 78 as follows:

> "if the number of errors is large (e.g. ≥ 4 bit errors) (66/76), it is concluded that the predicted IV is wrong (76), and appropriate action can be taken (78), which might consist of dropping crypto-sync and attempting to re-acquire it from the received IV (80)."

Although Gilley discloses that "an appropriate action" may be taken and that the appropriate action may consist of "dropping crypto-sync and attempting to acquire it from the received IV," nowhere does Gilley disclose "a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit" as recited in claim 1.

As further evidence that Gilley does not disclose a correction circuit as recited in claim 1, Gilley discloses at column 5, lines 21 – 30 that the preferred embodiment achieves a stated objective of maintaining crypto-sync (column 6, line 49) "without error correction." That is, the technique disclosed by Gilley does not involve error correction. Because the technique disclosed by Gilley does not involve error correction, Applicant asserts that Gilley does not disclose a correction circuit as recited in claim 1.

Dependent claim 2

Claim 2 recites that the correction circuit "comprises a circuit element that ***replaces the actual next bit with the corrected actual next bit*** in the plurality of bits." As stated above with regard to claim 1, Gilley does not disclose a correction circuit and Gilley explicitly states that the preferred embodiment achieves the stated objective of maintaining crypto-sync "without error correction." Because Gilley does not disclose error correction, it follows that the limitations of claim 2 which relate to error correction are not disclosed by Gilley.

In the Office action, Fig. 4, #74 and columns 6 – 7, lines 66 – 3 of Gilley are cited as disclosing the limitations of claim 2. Element 74 recites the phrase "use predicted IV to decrypt" while column 6, lines 66 – 67 states that "the predicted IV is used" to decrypt. Applicant respectfully asserts that using a predicted initialization

vector (IV) to decrypt does not anticipate a circuit that "replaces the actual next bit with the corrected actual next bit in the plurality of bits," as recited in claim 1.

Dependent claim 4

Claim 4 recites that the bit error detection circuit of claim 1 further includes "***a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected***." As stated above with regard to claim 1, Gilley does not disclose a correction circuit and Gilley explicitly states that the preferred embodiment achieves the stated objective of maintaining crypto-sync "without error correction." Because Gilley does not disclose error correction, it follows that a trigger circuit that activates a correction circuit is not disclosed by Gilley.

In the Office action, Fig. 4, #68 and column 6, lines 46 – 57 of Gilley are cited as disclosing the limitations of claim 4. Elements 64, 66, and 68 of Fig. 4 disclose that when no bit errors are detected, it should be assumed that the received and predicted initialization vectors are correct. These elements, particularly element 68, disclose nothing about a trigger circuit that "activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected" as recited in claim 4.

Dependent claims 5, 6, and 7

Dependent claims 5, 6, and 7 include limitations related to the trigger circuit. Because, as described above, Gilley does not disclose a correction circuit or a trigger circuit that activates the correction circuit, Applicant asserts that Gilley does not disclose the limitations related to the trigger circuit.

Claim 8

Claim 8 recites:

> "A bit error detection circuit comprising:
> a shift register that receives N bits of a pseudo-random bit sequence (PRBS);

a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit;

a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and

a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register. " (emphasis added)

Claim 8 is rejected under basically the same logic as claim 1. Because of the similarities between claims 1 and 8, Applicant asserts that the remarks provided above with reference to claim 1 apply also to claim 8.

Dependent claims 9 – 13

Dependent claim 9 has similar limitations to dependent claim 2 and therefore the remarks provided above with reference to claim 2 apply also to claim 9.

Dependent claim 10 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 10.

Dependent claims 11 and 12 include limitations related to the trigger circuit recited in claim 10. Because, as described above, Gilley does not disclose correction logic or a trigger circuit that activates the correction logic, Applicant asserts that Gilley does not disclose the limitations related to the trigger circuit.

Dependent claim 13 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 13.

Claims 14, 21, and 22

Claims 14, 21, and 22 include limitations that are similar to the limitations in claim 1. These claims are rejected under basically the same logic as claim 1. Because of the similarities between claims 1 and claims 14, 21, and 22, Applicant asserts that the remarks provided above with reference to claim 1 apply also to these claims.

Dependent claims 15 – 20

Dependent claim 15 has similar limitations to dependent claim 2 and therefore the remarks provided above with reference to claim 2 apply also to claim 15.

Dependent claim 17 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 17.

Dependent claims 16 and 18 – 20 are dependent on claim 14. Applicant asserts that these claims are allowable at least based on an allowable claim 14.

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
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Dated: January 23, 2006

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